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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,733	10/04/2000	Hideyuki Iino	1450.1006	6735
21171	7590	01/12/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			DAMIANO, ANNE L	
			ART UNIT	PAPER NUMBER
			2114	
DATE MAILED: 01/12/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

<b>Application No.</b>	09/678,733	<b>Applicant(s)</b>	
	Examiner Anne L Damiano	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) Responsive to communication(s) filed on Amendment filed 10/22/03.
- 2a) This action is FINAL.                  2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) Claim(s) 1-12 and 14-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 10-12 and 14-16 is/are allowed.
- 6) Claim(s) 1,3,4,6 and 7 is/are rejected.
- 7) Claim(s) 2,5,8 and 9 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 October 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) The translation of the foreign language provisional application has been received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- |  |  |
|--|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                               | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)           | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ .                                   |

**DETAILED ACTION**

***Drawings***

1. The corrected drawings were received on 10/22/03. These drawings are acceptable.

***Allowable Subject Matter***

2. Claims 2, 5, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
3. Claims 10-12 and 14-16 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of claims 10-12 is the inclusion of a reset selection section for outputting a system reset signal supplied to both a central processing section and a peripheral control section, one of an external reset signal and an emulator signal based on a reset instruction from the emulator, in a reset control system having a central processing section and a peripheral control section formed on separate chips, as recited in the claims.

The primary reason for allowance of claims 14 and 15 is the inclusion of masking an external reset signal when an emulator that independently implements a function of

the central processing section is in operation and supplying the reset signal to both chips of the central processing section and the peripheral control section, in a reset control method of a system having a central processing section and a peripheral control section formed on separate chips, as recited in the claims.

The primary reason for allowance of claim 16 is the inclusion of a reset selection section for outputting a system reset signal supplied to both a central processing section and a peripheral control section, one of an external reset signal and an emulator signal based on a reset instruction from the emulator, in a reset control method of a system having a central processing section and a peripheral control section formed on separate chips, as recited in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 4, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Mueller (6,226,756).

As in claim 1, Mueller discloses a reset control system of a system having a central processing section (figure 3: component 310) and a peripheral control section which are formed on separate chips (figure 1: components 102, 112 and 114, column 3: lines 9-24) (The system logic, controlling the I/O bus 112, which transfers data to an I/O device or a processor, lines 17-19, is interpreted as a peripheral control section on a separate chip as the central processing system) said reset control system comprising:

An emulator (figure 3: component 305);

A system reset output section generating and outputting a system reset signal on the basis of an external reset signal (column 7: lines 49-62) (push-button reset) and an emulator reset signal based on a reset instruction from the emulator to independently

implement a function of the central processing section (column 7: line 63-column 8: line 3 and figure 3),

Wherein the system reset signal output from the system output section is supplied to both chips of the central processing section and the peripheral control section. (Figure 3: components 315, 310, figure 1, components 108, column 7: line 63-column 8: line 3, column 8: line 63-column 9: line 3 and table 3, RSTOUT signal description (column 90: approximately lines 44-46)). (A hard reset initializes the system logic and processor to a predetermined state (column 7: lines 49-50). The system logic controls the I/O devices or peripheral devices, (Figure 1: components 108, 112, 114 and 116) the reset of the system logic is interpreted as being a reset of the peripheral control system. A push-button can trigger a hard reset (column 7: lines 55-57). Therefore, when a system reset signal is outputted on the basis of the external reset signal of the push-button, the reset signal must be supplied to both the central processing section and the peripheral control section. The output of the reset circuit of the emulator resets the processor and the peripheral control system.)

As in claim 4, Mueller discloses the system reset output section being provided in the chip of the central processing section (figure 3: components 315, 370 and 310).

As in claim 6, Mueller discloses the reset control system further comprising a synchronization processing section for synchronizing activation timing after reset between the central processing section and the peripheral control section, with the

synchronization processing section being formed on the chip of the central processing section (figure 4: component 410 and column 11: lines 40-53).

As in claim 7, Mueller discloses the synchronization processing section comprising an activation enable signal output section for output section for instructing to enable activation after elapse of a predetermined time after reset of the central processing section of the peripheral control section (column 8: lines 58-67, column 10: lines 11-13 and lines 49-65). (The hard reset to system logic, occurring at a certain time, synchronously with the system clock, caused by the RSTOUT signal from the reset circuit, is interpreted as enable activation after elapse of a predetermined time after reset of the central processing section.)

#### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller as applied to claim 1 above.

Regarding claim 3, Mueller discloses the claimed invention except for the system reset output section is provided in the chip of the central processing section (figure 3: components 315, 370 and 310).

It would have been obvious to a person skilled in the art at the time the invention was made to put the system reset output section in the chip of the peripheral control section, since it is held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

#### ***Response to Arguments***

7. Applicant's arguments filed 10/22/03 with respect to claim 1 have been fully considered and are not persuasive.

The examiner respectfully submits that Mueller teaches the limitations recited in claim 1.

The system logic controls the I/O devices or peripheral devices and is therefore interpreted as equivalent to a peripheral control section (Figure 1: components 108, 112, 114 and 116 and column 3: lines 9-24) and as existing on a separate chip as the central processing section.

Mueller discloses that a push-button, an external signal, can trigger a hard reset. The hard reset initializes the peripheral control section (control logic) and the central processing section (processor) to a predetermined state (column 7: lines 49-50). Therefore, when a system reset signal is outputted on the basis of the external reset

signal of the push-button, some signal must be supplied to both the central processing section and the peripheral control section, in order for each to be initialized in accordance with a hard reset. This signal being supplied to both means that Mueller's invention teaches the limitation of the system reset signal being supplied to separate chips.

Rejection of claim 2 has been withdrawn.

Applicant's arguments with respect to claim 3 have been fully considered and are not persuasive.

See claim rejection above.

The examiner maintains the original rejection of dependent claims 4, 6 and 7.

See claim rejection above.

Applicant's arguments with respect to dependent claim 5 have been fully considered and are persuasive. Therefore, the rejection of this claim, as well was its dependent claims, 8 and 9, has been withdrawn.

Applicant's arguments with respect to independent claims 10, 14 and 16 have been fully considered and are persuasive. Therefore, the rejection of these claims, as well as their dependent claims, 11, 12 and 15 has been withdrawn.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Art Unit: 2184

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ALD



**SCOTT BADERMAN**  
**PRIMARY EXAMINER**